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EXAMINER	
WONG, LINDA	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/678,685	DOUMA ET AL.	
	Examiner	Art Unit	
	LINDA WONG	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 May 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-24 and 26-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-24 and 26-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application.
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments filed 5/25/2010 have been fully considered but they are not persuasive.

   a. Regarding claim 1, the applicant contends Lutz fails to disclose the limitation "the timing circuit including a comparator that compares a first reference signal with a signal from the capacitor and resistor network used to measure the period of time that the synchronization signal is asserted, the comparator outputting the lock signal based on the comparison."

      The examiner respectfully disagrees. Fig. 3a, label 16, timing circuit, shows an operational amplifier or comparator, label 300, for receiving the synchronization signal, label 44, and comparing the signal with a reference signal, input to label +. Col. 8, lines 8-15 discloses "lacking the random excursions, the signal will no longer cause the potential developed at the inverting input of the operational-amplifier 300 to exceed the potential developed at its non-inverting input." This indicates amplifier 300 acts as a comparator to ensure the inverting input does not exceed a potential at the non-inverting input./ Fig. 3a, label 16 shows a network of capacitors and resistors connected to the comparator or operational amplifier, label 300. Col. 7, line 40 - Col. 8, line 22 discloses the lock detector and timer 16 determines if the noisy, hunting signal is relatively constant. Capacitor and resistor (304,308,310) are time constant components. The PLL is stable or synchronized when the signal at line 44 is constant. The operation amplifier 300 will compare the

synchronization signal with a reference input. The capacitor inherently charges till a period of time. The resistor prolongs the time in which the capacitor will stay in charge mode. The capacitor and resistor network will inherently measure an amount of time line 44 is constant and the PLL is synchronized.)

b. Regarding claim 19, the applicant contends

"Claim 19 recites, among other things, "a timing circuit adapted to measure a period of time that the synchronization signal is asserted using at least a capacitor arranged to discharge when the synchronization signal is asserted and to charge when the synchronization signal is not asserted." The Examiner first identified a capacitor (318) in *Lutz* as the claimed capacitor. *See Office Action* at 8 and 9 (citing *Lutz* at column 8, lines 19-22). However, the Examiner later identified a different capacitor (360) in *Lutz* as the claimed capacitor that is "arranged to discharge when the synchronization signal is asserted and to charge when the synchronization signal is not asserted." *See id.* (citing *Lutz* at column 8, lines 55-67, which refers to "discharge capacitor 360"). Both capacitors cannot logically correspond to the claimed "a capacitor."

In fact, capacitor (318) is part of a first timer (16) that "develop[s] on a line 46 a (stabilization signal) of predetermined period after [a] lock signal has stabilized," whereas capacitor (360) is part of a second timer (18) that "responds to the delayed lock signal developed on line 46...[and] causes the state of [a] reset signal to change and, a predetermined time thereafter, it causes the state of [a] latch signal to change." *See Lutz* at col. 3, line 56, through col. 4, line 2, and Figure 1. Therefore, the capacitors are used in different timers for different purposes and are not both used by a single timing circuit (or timer) to "measure a period of time that the synchronization signal is asserted," as claimed.

Applicants respectfully note that while the foregoing points with respect to claim 19 were raised in Applicants previous response, the Examiner has failed to take note of and address these points, contrary to MPEP guidance.

In light of the foregoing, Applicants respectfully submit that no *prima facie* case of anticipation has been established with respect to claim 19. Accordingly, Applicants respectfully request withdrawal of the rejection of claim 19, and corresponding dependent claims 20-24, 26, and 28.

The examiner respectfully disagrees. The examiner has cited Col. 8, lines 45-67, wherein such lines describe both operational amplifiers 360 and 340. The column describes the relationship between the amplifiers 340 and 360 as the capacitors 318, 360 charge and discharge respectively. Col. 8, lines 45-67 describes capacitor 318 charges when the PLL is in a state of synchronization, simultaneously, capacitor 360 discharges. Even though Lutz only discloses a

scenario when the PLL is synchronized, capacitors will eventually change its state from discharge to charge and vice versa. Since Lutz discloses capacitor 318 charges when the PLL is synchronized, the capacitor 318 will discharge once the PLL is not asserted or no longer in synchronization. When the PLL is not in a state of synchronization, capacitor 360 will charge.

c. Regarding **claims 3,4,6-8,20-24,26,28**, such claims are dependent on respective independent claims. Please see the rebuttal of the independent claim.

d. Regarding **claims 9,13,29,14,18**, such claims are dependent on amended claims. Please see the rejection below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 1-3,6-7, 9-12,19-20,24-26,28,29** are rejected under 35 U.S.C. 103(a) as being unpatentable over Khoury, Jr. et al (US Publication No.: 20040042504) in view of Lutz (US Patent No.: 4276548).

a. **Claim 1**, Khoury, Jr. et al disclose

- "a demultiplexer arranged to receive a clock signal from the phase locked loop, the demultiplexer being configured to convert the serial data signal to

a parallel data signal based on the clock signal." (Fig. 2, label 48a as the demux and label ck1 as the clock from the phase locked loop, wherein label 48a outputs parallel signals Dout1 and Dout2.)Lutz discloses:

- Khour, Jr. et al fails to disclose the limitations of the PLL.

ii. Lutz discloses

- "a controller chip that includes a phase locked loop adapted to operate in a hunting mode and a locked mode" (Fig. 1, label 10 shows the controller chip, label 14 as the phase locked loop, Col. 3, lines 49-65 discloses the hunting period occurs when the output on line 44 is random or noisy nature and the lock detector and timer senses the random nature of the synchronization signal, label 44 as shown in Fig. 1.)
- "wherein, the phase locked loop is further adapted to assert a synchronization signal in the hunting mode when a hunting frequency passes through a data signal frequency" (Col. 3, lines 49-55 discloses hunting occurs when the synchronization of the frequency of the internal oscillator is not synchronized with the frequency of a coherent component of the difference signal.)
- "wherein the phase locked loop is further adapted to keep the synchronization signal asserted as long as the phase locked loop is locked onto a data signal" (Col. 3, lines 49-65 discloses the phase locked loop outputs a constant level DC signal when the is synchronized. "Lock detector and timer includes suitable circuitry for sensing the random nature

of the lock signal and for developing on the line a stabilization signal of predetermined period after the lock signal has stabilized.")

- "a timing circuit adapted to measure a period of time that the synchronization signal is asserted using a capacitor and resistor network and to produce a lock signal if the synchronization signal is asserted for at least a specified period of time" (Fig. 1, label 16 shows a lock detector and timer. Col. 3, lines 49-65 disclose "Lock detector and timer includes suitable circuitry for sensing the random nature of the lock signal and for developing on the line a stabilization signal of predetermined period after the lock signal has stabilized." Fig. 3a, label 16, timing circuit, shows an operational amplifier or comparator, label 300, for receiving the synchronization signal, label 44, and comparing the signal with a reference signal, input to label +. Col. 8, lines 8-15 discloses "lacking the random excursions, the signal will no longer cause the potential developed at the inverting input of the operational-amplifier 300 to exceed the potential developed at its non-inverting input." Fig. 3a, label 16 shows a network of capacitors and resistors connected to the comparator or operational amplifier, label 300. Col. 7, line 40 - Col. 8, line 22 discloses the lock detector and timer 16 determines if the noisy, hunting signal is relatively constant. Capacitor and resistor (304,308,310) are time constant components. The PLL is stable or synchronized when the signal at line 44 is constant. The operation amplifier 300 will compare the synchronization

signal with a reference input. The capacitor inherently charge and discharge for periods of time. The resistor prolongs the time in which the capacitor will stay in charge mode. The capacitor and resistor network will inherently measure an amount of time line 44 is constant and the PLL is synchronized.) It would have been obvious to one skilled in the art at the time of the invention to use a PLL as disclosed by Lutz et al in the clock data recovery for controlling the demultiplexer as disclosed by Khoury, Jr. et al so to efficiently synchronize an input signal with the internal clock, thus producing a clock output that will match the data rate of the input signal.

b. **Claim 2**, Lutz discloses "the timing circuit is an analog timer comprising a capacitor and resistor network." (Fig. 3a, label 16 shows the lock detector and timer, wherein the block has a network of resistors and capacitors.)

c. **Claim 3**, Lutz discloses "the timing circuit comprises a transistor for resetting the timing circuit" (Fig. 1, label 18 is a timer for resetting the timing circuit, label 16, wherein the timer has a transistor, label 342.)

d. **Claim 6,** Lutz discloses "an input level detector that compares the synchronization signal with a reference signal and produces logical signals within the timing circuit". (Fig. 3a, label 16, timing circuit, shows an operational amplifier or comparator, label 300, for receiving the synchronization signal, label 44, and comparing the signal with a reference signal, input to label +. Col. 8, lines 8-15 discloses "lacking the random excursions, the signal will no longer

cause the potential developed at the inverting input of the operational-amplifier 300 to exceed the potential developed at its non-inverting input.")

e. **Claim 7**, Lutz discloses "wherein the timing circuit outputs the lock signal to a host device". (Fig. 3a, label 46 is outputted to timer 18, which controls the display as shown in Fig. 3b. Line 46 determines after a period of time, the PLL is synchronized. (Col. 8, lines 20-23))

f. **Claim 9**,

i. Khoury, Jr. et al disclose a PLL or clock data recovery unit for synchronizing a data signal with a data frequency "corresponding to a rate of data encoded in a data signal". (Paragraph 27 discloses the PLL recites the data signal. Since the PLL synchronizes using the data signal, wherein the data signal comprises its own data rate, the data frequency would correspond to the data rate of the data signal.)

ii. Khoury, Jr. et al fail to disclose the limitations of the PLL.

iii. Lutz discloses

- "an output adapted to couple to a host device" (Fig. 1, labels 22,24 as the output, label 10 as the host device.)
- "a controller chip having a phase locked loop that is adapted to operate in a hunting mode" (Fig. 1, label 10 (PLL and connected components) shows the controller chip, label 14 as the phase locked loop, Col. 3, lines 49-65 discloses the hunting period occurs when the output on line 44 is random or

noisy nature and the lock detector and timer senses the random nature of the synchronization signal, label 44 as shown in Fig. 1.)

- Hunting mode "in which the phase locked loop briefly asserts a synchronization signal when a hunting frequency passes through a data signal frequency". (Col. 3, lines 49-55 discloses hunting occurs when the synchronization of the frequency of the internal oscillator is not synchronized with the frequency of a coherent component of the difference signal.)
- "and the phase locked loop also being adapted to operate in a locked mode in which the phase locked loop asserts the synchronization signal so long as the phase locked loop is locked onto a data signal" (Col. 3, lines 49-65 discloses the phase locked loop outputs a constant level DC signal when the is synchronized. "Lock detector and timer includes suitable circuitry for sensing the random nature of the lock signal and for developing on the line a stabilization signal of predetermined period after the lock signal has stabilized.")
- "a translation circuit including:
- "a level detector that compares the synchronization signal with a first reference signal to produce a logical signal based on the comparison" (Fig. 3a, label 300 for comparing the synchronization signal 44 with a non-inverted signal. Col. 8, lines 8-15 discloses "lacking the random excursions, the signal will no longer cause the potential developed at the inverting input

of the operational-amplifier 300 to exceed the potential developed at its non-inverting input.")

- "a timer adapted to measure a period of time that the logical signal is asserted to produce a timer signal" (Fig. 3a, labels 310,304,308,316,318 are capacitors and resistor connections, wherein such components will inherently measure a period of time. The capacitor will discharge/charge after a period of time and the resistor limits or prolongs the amount of time in which the capacitors will charge and discharge.)
- "a comparator that compares the timer signal with a second reference signal to produce a lock signal for use by the host device" (Fig. 3b, label 46 as the stabilization signal, which is measured by the lock detector to determine if the PLL is locked after a period of time found by label 16 of Fig. a. Line 46 is compared to a second reference signal (Fig. 3b, label 340).
- "wherein a logic level of the lock signal is asserted when the phase locked loop is locked onto a data signal for a period of time measured by the timer and is de-asserted when the phase locked loop asserts the synchronization signal in hunting mode." (Fig. 1, label 16 shows a lock detector and timer. Col. 3, lines 49-65 disclose "Lock detector and timer includes suitable circuitry for sensing the random nature of the lock signal and for developing on the line a stabilization signal of predetermined period after the lock signal has stabilized." Lines 49-55 disclose the hunting mode occurrence. Fig. 3a, label 16 measures the amount of time line 44 is stable before

declaring locked condition of the PLL. (Col. 3, lines 56-65)) It would have been obvious to one skilled in the art at the time of the invention to use a PLL as disclosed by Lutz et al in the clock data recovery as disclosed by Khoury, Jr. et al so to efficiently synchronize an input signal with the internal clock, thus producing a clock output that will match the data rate of the input signal.

g. **Claim 10**, Lutz discloses "the translation circuit comprising a timer adapted to measure a period of time that the synchronization signal is asserted." (Fig. 1, label 16 and 18 for resetting the timing.)

h. **Claims 11,12**, Lutz discloses "an input level detector that compares the synchronization signal with a reference signal and produces logical signals within the timing circuit". (Fig. 3a, label 16, timing circuit, shows an operational amplifier or comparator, label 300, for receiving the synchronization signal, label 44, and comparing the signal with a reference signal, input to label +. Col. 8, lines 8-15 discloses "lacking the random excursions, the signal will no longer cause the potential developed at the inverting input of the operational-amplifier 300 to exceed the potential developed at its non-inverting input.")

i. **Claim 19**, Lutz discloses

- "a timing circuit adapted to measure a period of time that the synchronization signal is asserted using at least a capacitor, wherein the timing circuit is further adapted to generate an output signal having a voltage across the capacitor" (Col. 3, lines 55-60 discloses "Lock detector

and timer 16 includes suitable circuitry for sensing the random nature of the lock signal and for developing on a line 46 a (stabilization signal) of predetermined period after the lock signal has stabilized." Col. 8, lines 8-15 discloses "lacking the random excursions, the signal will no longer cause the potential developed at the inverting input of the operational-amplifier 300 to exceed the potential developed at its non-inverting input." Col. 8, lines 19-22 discloses "A predetermined time after synchronization is achieved, the potential developed across capacitor 318 will rise to a level which will trigger timer 18 ..." Fig. 3a, label 318 shows the Voltage of the output would be across the such a capacitor. Fig. 3b, label 18 shows the timer, which sends information to label 16, Fig. 3a, through label E.)

- "a comparator circuit adapted to compare the output signal with a reference signal such that a lock signal is not asserted unless the comparison of the output signal with the reference signal indicates that the period of time that the synchronization signal is asserted exceeds a minimum period of time" (Col. 3, lines 55-60 discloses "Lock detector and timer 16 includes suitable circuitry for sensing the random nature of the lock signal and for developing on a line 46 a (stabilization signal) of predetermined period after the lock signal has stabilized." Col. 8, lines 8-15 discloses "lacking the random excursions, the signal will no longer cause the potential developed at the inverting input of the operational-amplifier 300 to exceed the potential developed at its non-inverting input.")

- Wherein the capacitor is "arranged to discharge when the synchronization signal is asserted and to charge when the synchronization signal is not asserted" (Col. 8, lines 55-67 discloses when the PLL synchronizes the internal clock with the data signal, the capacitor discharges. Since the capacitor discharges when the PLL is synchronized, the capacitor would charge when the PLL is hunting.)

j. **Claim 20**, Lutz discloses "the timing circuit comprises a transistor that is controlled by the synchronization signal for resetting the timing circuit such that the capacitor discharges." (Fig. 1, label 18 is a timer for resetting the timing circuit, label 16, wherein the timer has a transistor, Fig. 3b, label 342. Fig. 3a, label 16 shows the synchronization signal controls the lock detector and timing component, label 16. Based on the information from the synchronization signal, label 16 outputs information to label 18, timer, where the transistor determines resetting mode.)

k. **Claim 24**, Lutz discloses "an input level detector that passes the synchronization signal to the timing circuit when the synchronization signal exceeds a reference voltage." (Col. 3, lines 55-60 discloses "Lock detector and timer 16 includes suitable circuitry for sensing the random nature of the lock signal and for developing on a line 46 a (stabilization signal) of predetermined period after the lock signal has stabilized." Col. 8, lines 8-15 discloses "lacking the random excursions, the signal will no longer cause the potential developed at the inverting input of the operational-amplifier 300 to exceed the potential

developed at its non-inverting input." Col. 8, lines 19-22 discloses "A predetermined time after synchronization is achieved, the potential developed across capacitor 318 will rise to a level which will trigger timer 18 ..." Fig. 3a, label 318 shows the Voltage of the output would be across the such a capacitor.)

l. **Claim 28**, Lutz discloses "the capacitor is arranged such that a voltage across the capacitor is an average of the synchronization signal over a period of time". (Col. 9, lines 12-25, discloses when line 352 is low, the capacitor is charging for a predetermined time. Col. 8, lines 8-22, discloses the timer 18 is triggered after a period of time where synchronization has been achieved. Col. 8, lines 55-64 discloses the synchronization state of the PLL causes a low potential on line 352, and as discussed above, line 352 determines the charging of the capacitor. When the state is changed, line 352 is changed. Thus, the predetermined amount of time the capacitor is charging depends on the amount of time synchronization is achieved. Thus, the voltage across the capacitor would be an average of the synchronization signal over a period of time.)

m. **Claim 29**, Khoury, Jr. et al discloses "the data encoded in the data signal is digital data encoded with data encoding circuitry." (Paragraph 1 discloses aligning data bits, wherein paragraph 2 discloses transmission of the data bits (digital data) from a transmitter to receiver. Khoury, Jr. et al's invention receivers data bits through a data channel from a transmitter, the transmitter will encode the data bits in the signal prior to transmission. Example of such a

transmitter is Patent No.: 5079770 or 20030195645. An encoder is inherent in the transmitter that sends data bits over a data channel.)

3. **Claims 14-16,27,30** are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (pages 2-5) in view of Lutz (US Patent No.: 4276548).

   a. **Claim 14**,

      i. Regarding the limitations, "in response to the asserted lock signal, sampling data from the data signal" and "extracting a clock signal from the data signal" and "using the extracted clock signal as a reference for converting the sampled signal into synchronized data to be read by the host device", The admitted prior art discloses a microcontroller for sampling the data, extracting a clock signal from the data, using the clock as a reference for synchronizing the data, wherein the synchronization is performed using a PLL as described in paragraphs 6 and 7. Paragraph 6 discloses "once the clock is extracted and the data is sampled ..." This indicates an asserted clock is used for sampling the data signal.)

      ii. The admitted prior art fails to disclose all the PLL functionalities.

      iii. Lutz discloses

      - receiving a synchronization signal from a phase locked loop, the phase locked loop disposed on the controller chip (Fig. 1, label 10 shows the controller chip, label 44 as the synchronization signal outputted from label 14, phase locked loop.);

- "obtaining an average of the synchronization signal over a period of time" (Fig. 1, label 16 receives a PLL development signal from line 44 of Fig. 3a and measures over a period of time whether the signal on line 44 is stable. (Col. 3, lines 55-65))
- "comparing the average of the synchronization signal with a reference signal to determine whether the synchronization signal is caused by the phase locked loop locking onto a data signal or by the phase locked loop passing a hunting frequency through a data signal frequency (Col. 3, lines 49-65 discloses the hunting period occurs when the output on line 44 is random or noisy nature and the lock detector and timer senses the random nature of the synchronization signal, label 44 as shown in Fig. 1. Fig. 3a, line 46 is compared to a reference signal shown in Fig. 3b, label 340. Col. 3, lines 55-65 discloses determining whether the signal on line 46 has been stabilized over a period of time.)
- asserting a lock signal if the phase locked loop has locked onto the data signal (Col. 3, lines 55-60 discloses the lock detector and timer determines whether the synchronization signal is stabilized after a predetermined period.) It would have been obvious to one skilled in the art at the time of the invention to use a PLL as disclosed by Lutz in the admitted prior art for sampling data signal so to effectively monitor the condition of the PLL and the state of synchronization, thus reducing cost and allows for accurate detection of when a frequency/phase difference has occured.

b. **Claim 15**, Lutz discloses

i. "measuring a period of time that the synchronization signal is asserted" (Col. 8, lines 8-15 discloses "lacking the random excursions, the signal will no longer cause the potential developed at the inverting input of the operational-amplifier 300 to exceed the potential developed at its non-inverting input.")

ii. "determining that the synchronization signal is caused by the phase locked loop locking onto the data signal if the period of time that the synchronization signal is asserted is greater than a specified period of time." (Col. 3, lines 55-60 discloses "Lock detector and timer 16 includes suitable circuitry for sensing the random nature of the lock signal and for developing on a line 46 a (stabilization signal) of predetermined period after the lock signal has stabilized.")

c. **Claim 16**, Lutz discloses "comparing the asserted synchronization signal with a reference signal to determine if the asserted synchronization signal is produced by the phase locked loop locking onto a data signal or by the phase locked loop passing a hunting frequency through the data signal frequency." (Col. 3, lines 55-60 discloses "Lock detector and timer 16 includes suitable circuitry for sensing the random nature of the lock signal and for developing on a line 46 a (stabilization signal) of predetermined period after the lock signal has stabilized." Col. 3, lines 49-55 describes the hunting mode.)

d. **Claim 27**, the admitted prior art discloses "wherein the data signal is an electronic data signal, the fiber-optic transponder further comprising circuitry to convert optical data signal to the electronic data signal". (Paragraph 3) It would have been obvious to one skilled in the art to combine the components found in Lutz as discussed in claim 9 and components of a fiber optical transponder as disclosed by the admitted prior art so provide information to a computer using fiber optic cables so to provide efficient synchronization within a computer system.

e. **Claim 30**, Lutz discloses "wherein obtaining the average includes creating a time lag between when a change occurs in the synchronization signal and when the change is taken into account by the average of the synchronization signal." (Col. 7, line 55-Col. 8, line 7 discloses the use of a potentiometer to determine when the signal on line 44 is noisy and hunting over a period of time. The amplifier will indicate the reference potential generated at its non-inverting point has been exceeded.)

4. **Claim 4** is rejected under 35 U.S.C. 103(a) as being unpatentable over Khoury, Jr et al in view of Lutz as applied to claim 1, in view of Transistors Non-Patent Literature.

a. **Claim 4**, Lutz fails to disclose the type of transistors used in his timer, however, Transistors Non-Patent Literature discloses transistor is at least one of a PNP and NPN bipolar junction transistor (p. 3, The NPN Transistor). Because NPN

transistor are well known in the art as low cost transistor with low power consumption at low voltage levels, it would have been obvious to one skilled in the art at the time of invention to incorporate a NPN transistor as disclosed by Transistors Non-Patent Literature into the combined invention disclosed by Lutz.

5. **Claim 21** is rejected under 35 U.S.C. 103(a) as being unpatentable over Khoury, Jr et al in view of Lutz as applied to claim 19, in view of Transistors Non-Patent Literature.
   a. **Claim 21**, Lutz fails to disclose the type of transistors used in his timer, however, Transistors Non-Patent Literature discloses transistor is at least one of a PNP and NPN bipolar junction transistor (p. 3, The NPN Transistor). Because NPN transistor are well known in the art as low cost transistor with low power consumption at low voltage levels. It would have been obvious to one skilled in the art at the time of invention to incorporate a NPN transistor as disclosed by Transistors Non-Patent Literature into the combined invention disclosed by Lutz.

6. **Claim 26** is rejected under 35 U.S.C. 103(a) as being unpatentable over Khoury, Jr et al in view of Lutz as applied to claim 19.
   a. **Claim 26**, Lutz discloses

- "the capacitor is coupled to the transistor such that current flows through the transistor to charge the capacitor when the synchronization signal is not asserted at a rate faster than a rate at which the capacitor discharges through a resistor coupled thereto" (Fig. 3b, label 342 as the transistor, label 360 as the capacitor, Col. 8, lines 45-67 describes the functionality of the circuit shown in Fig. 3b, label 18. Col. 8, lines 64-67 discloses the transistor provides a path to discharge the capacitor when the PLL has synchronized the data signal to the internal clock. This indicates the capacitor will charge when the synchronization signal is not asserted. As described in Col. 8, lines 45-67, when the potential on label 352 is high, the transistor is saturated, causing the transistor to act as a short. A certain amount of current will pass through the shorted line as well as the capacitor. When the potential on line 352 is low, the transistor is turned off or the switch is open. The total amount of current will pass through the capacitor, thus the capacitor will charge at a higher rate than the discharge rate.)
- "the comparator circuit is adapted to assert the lock signal when the voltage across the capacitor exceeds the reference signal" (Col. 3, lines 55-60 discloses "Lock detector and timer 16 includes suitable circuitry for sensing the random nature of the lock signal and for developing on a line 46 a (stabilization signal) of predetermined period after the lock signal has stabilized." Col. 8, lines 8-15 discloses "lacking the random excursions, the

signal will no longer cause the potential developed at the inverting input of the operational-amplifier 300 to exceed the potential developed at its non-inverting input.")

- Lutz uses a NPN transistor wherein it would have been obvious to one skilled in the art to use a PNP transistor since the functionality of a PNP is the inverse of the NPN and can perform the same functionalities, thus allowing the circuit as soon in Fig. 3b to provide timing information, wherein the timing information would efficient locking information.

7. **Claim 17** is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Lutz as applied to claim 14, in view of Rumbaugh (US Patent No. 6275144).

   a. **Claim 17,**

      i. Lutz discloses "comparing the lock signal with a reference signal to produce the lock signal useful by a host device". (Fig. 3a, label 16, timing circuit, shows an operational amplifier or comparator, label 300, for receiving the synchronization signal, label 44, and comparing the signal with a reference signal, input to label +. Col. 8, lines 8-15 discloses "lacking the random excursions, the signal will no longer cause the potential developed at the inverting input of the operational-amplifier 300 to exceed the potential developed at its non-inverting input." Fig. 1, labels 22,24,12 shows the host device.)

ii. Lutz fails to disclose the host device is connected to a fiber optic transponder.

iii. Rambaugh discloses connection using fiber optics. (Fig. 3 shows the connections. Col. 4, lines 39-41 discloses a fiber optic interface device.) It would have been obvious to one skilled in the art at the time of the invention to connect the system as shown by Lutz to a fiber optics device as shown by Rumbaugh so to provide better and quicker transmission.

8. **Claim 8** is rejected under 35 U.S.C. 103(a) as being unpatentable over Lutz in view of Khourdy, Jr et al as applied to claim 7, further in view of IBM Technical Disclosure Bulletin, May 1990.

a. **Claim 8**,

i. Lutz fail to disclose a comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value.

ii. IBM Technical Disclosure Bulletin, May 1990 discloses a comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value (see part 3 and figure 2). The disclosure further states that this scheme has the advantage of providing a stabilized synchronization acquisition (part 3, lines 2-3). Because of this advantage it would have been obvious to one skilled in the art a the time of

invention to incorporate the phase lock as disclosed by the IBM Technical Disclosure Bulletin, May 1990 into the combined invention of Lutz and Lee.

9. **Claims 13,22,23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Khoury, Jr. et al in view of Lutz as applied to claims 12,19, respectively, in view of IBM Technical Disclosure Bulletin, May 1990.

   a. **Claim 13**, Khoury, Jr. et al and Lutz fails to disclose a comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value. However, IBM Technical Disclosure Bulletin, May 1990 discloses a comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value (see part 3 and figure 2). The disclosure further states that this scheme has the advantage of providing a stabilized synchronization acquisition (part 3, lines 2-3). Because of this advantage it would have been obvious to one skilled in the art a the time of invention to incorporate the phase lock as disclosed by the IBM Technical Disclosure Bulletin, May 1990 into the combined invention of Lutz and Lee.

   b. **Claims 22, 23**, Khoury, Jr. et al and Lutz fails to disclose a comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value. However, IBM Technical Disclosure Bulletin, May

1990 discloses a comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value (see part 3 and figure 2). The disclosure further states that this scheme has the advantage of providing a stabilized synchronization acquisition (part 3, lines 2-3). Because of this advantage it would have been obvious to one skilled in the art a the time of invention to incorporate the phase lock as disclosed by the IBM Technical Disclosure Bulletin, May 1990 into the combined invention of Lutz.

10. **Claim 18** is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Lutz as applied to claim 14, respectively, in view of IBM Technical Disclosure Bulletin, May 1990.

    a. **Claim 18**, The admitted prior art and Lutz fails to disclose a comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value. However, IBM Technical Disclosure Bulletin, May 1990 discloses a comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value (see part 3 and figure 2). The disclosure further states that this scheme has the advantage of providing a stabilized synchronization acquisition (part 3, lines 2-3). Because of this advantage it would have been obvious to one skilled in the

art a the time of invention to incorporate the phase lock as disclosed by the IBM Technical Disclosure Bulletin, May 1990 into the invention of Lutz.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
    a. Meltzer (US Publication No.: 20030112915)
    b. Lee (US Publication No.: 20020094054)
    c. Eom (US Publication No.: 20020084859)
    d. Nishimura et al (US Patent No.: 6392641)
    e. Knechtel (US Patent No.: 4933959)
    f. Francis (US Patent No.: 5541556)
    g. Yamaguchi et al (US Patent No.: 4535306).

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

13. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then

the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LINDA WONG whose telephone number is (571)272-6044. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on (571) 272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Linda Wong/
Examiner, Art Unit 2611

/David C. Payne/

Supervisory Patent Examiner, Art Unit 2611